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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,404	11/28/2000	Hidekazu Takata	3917-2	4573

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EXAMINER	
ABRISHAMKAR, KAVEH	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,404	TAKATA ET AL.	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Request for Continued Examination (RCE) filed on June 10, 2005. Per the received RCE, claims 1,7,8,9,14,19, and 28, have been amended. Claims 1-32 are currently being considered.

Response to Arguments

2. Applicant's arguments, see RCE filed June 10, 2005 with respect to the rejection(s)of claim(s) 1-32 under Takata (U.S. Patent No. 6,594,777) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hsu (U.S. Patent No. 5,754,647) in view of Takata (U.S. Patent No. 6,594,777).

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 11-14, 16-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu (U.S. Patent No. 5,754,647).

Regarding claim 1, Takata discloses:

A semiconductor memory device storing regular data and having a security function for preventing unauthorized use of the regular data the semiconductor storage device configured for removable connection to a video game system including a video game program executing system and comprising:

a first store including a first storing area for fixedly storing a first portion of the regular data and a dummy data storing area for fixedly storing dummy data in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations);

a second store including a second storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the fist store and fixedly stores the second portion of the regular data (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations), and wherein the second store of data is interpreted as being the block of memory with regular data which is not in the contiguous first block of memory of regular data;

a read control circuit which is electrically connected to the video game program executing system when the semiconductor storage device is connected to the video game system, the read control circuit comparing an input address input thereto from the video game program executing system with a dummy address corresponding to an

address space of the dummy data storing area, enabling reading of the first portion of the regular data from the first store when the input address and the dummy address do not correspond, and disables the reading of the first portion of the regular data and enabling the reading of the second portion of the regular data from the second store when the input address and the dummy address correspond (column line 59 – column 6 line 46), wherein trap address detector detects when an erroneous address (dummy address) is trying to be accessed on the address bus, and disables the reading of the regular data, and instead, outputs erroneous data, but if the address is in the correct address space (regular data address space) reading is allowed.

Regarding claim 7, Takata discloses:

A memory device storing an application program and having a security function for preventing unauthorized use of the application program, the memory device configured for removable connection to a video game system including a video game executing system comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data in place of a second portion of the application program, the second portion of the application program being necessary for use of the application (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the second portion of the application program (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations), and wherein the second store of data is interpreted as being the block of memory with regular data which is not in the contiguous first block of memory of regular data; and

a read control circuit which is electrically connected to the video game program executing system when the electronic device is connected to the video game system, the read control circuit comparing an input address input from the video game program executing system with a dummy address corresponding to an address space of the dummy data storing area, enabling reading of the first portion of the application program from the first store when the input address and the dummy address do not correspond and disabling the reading of the first portion of the application program and enabling the reading of the second portion of the application program from the second store when the input address and the dummy address correspond (column line 59 – column 6 line 46), wherein trap address detector detects when an erroneous address (dummy address) is trying to be accessed on the address bus, and disables the reading of the regular data, and instead, outputs erroneous data, but if the address is in the correct address space (regular data address space) reading is allowed.

Regarding claim 8, Takata discloses:

An electronic device for storing an application program and having a security function for preventing unauthorized use of the application program, the electronic device configured for removable connection to a video game system including a video game program executing system and comprising:

a first store including a first program storing area for fixedly storing a first portion of the application program and a dummy data in place of a second portion of the application program, the second portion being necessary for the use of the application program (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first store and fixedly stores the second portion of the application program (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations), and wherein the second store of data is interpreted as being the block of memory with regular data which is not in the contiguous first block of memory of regular data; and

a read control circuit which is electrically connected to the video game program executing system when the electronic device is connected to the video game system, the read control circuit comparing an input address input thereto from the video game

program executing system with a dummy data of an address space of the dummy data storing area, enabling reading of the first application program from the first store when the input address and the dummy address are not identical, and disabling the reading of the first application program and enabling the reading of the second application program from the second store when the input address and the dummy address are identical (column line 59 – column 6 line 46), wherein trap address detector detects when an erroneous address (dummy address) is trying to be accessed on the address bus, and disables the reading of the regular data, and instead, outputs erroneous data, but if the address is in the correct address space (regular data address space) reading is allowed.

Regarding claim 9, Takata discloses:

A memory device storing a game program and having a security function for preventing unauthorized use of the game program, the memory device configured for removable connection to a game machine including a video game program executing system and comprising:

a first store including a first program storing area for fixedly storing a first portion of the game program and a dummy data storing area for fixedly storing dummy data in place of a second portion of the game program, the second portion being necessary for use of the game program (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations);

a second store including a second program storing area which has a storage capacity equal to at least a storage capacity of the dummy data storing area of the first stores the second portion of the game program (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations), and wherein the second store of data is interpreted as being the block of memory with regular data which is not in the contiguous first block of memory of regular data; and

a read control circuit which is electrically connected to the video game program executing system when the memory device is connected to the video game system, the read control circuit comparing an input address input thereto from the video game program executing system with a dummy address corresponding to an address space of the dummy data storing area and enabling reading of the first portion of the game program from the first store when the input address and the dummy address do not correspond, and disabling the reading of the first portion of the game program and enabling the reading of the second portion of the game program from the second store when the input address and the dummy address correspond (column line 59 – column 6 line 46), wherein trap address detector detects when an erroneous address (dummy address) is trying to be accessed on the address bus, and disables the reading of the regular data, and instead, outputs erroneous data, but if the address is in the correct address space (regular data address space) reading is allowed.

Regarding claim 14, Takata discloses:

A method of preventing unauthorized use of regular data stored in a storage device configured for removable connection to a video game system including a video game program executing system, the method comprising:

storing in a first storage area of the storage device a first portion of the regular data and storing dummy data in a dummy data area of said first storage area in place of a second portion of the regular data, the second portion of the regular data being necessary for use of the regular data (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations);

storing in a second storage area of the storage device having a storage capacity equal to at least a storage capacity of the dummy data storing area of the first storage area the second portion of the regular data (column 5 line 59 – column 6 line 46), wherein a game machine does not typically access the entire address space of its memory, and certain designated address locations are not used (dummy address locations), and wherein the second store of data is interpreted as being the block of memory with regular data which is not in the contiguous first block of memory of regular data; and

comparing an input address from the video game program executing system with a dummy address corresponding to an address space of the dummy data storing area and enabling reading of the first portion of the regular data from the first storage area when the input address and the dummy address do not correspond and disabling the

reading of the first portion of the regular data and enabling the reading of the second portion of the regular data from the second storage area when the input address and the dummy address correspond (column line 59 – column 6 line 46), wherein trap address detector detects when an erroneous address (dummy address) is trying to be accessed on the address bus, and disables the reading of the regular data, and instead, outputs erroneous data, but if the address is in the correct address space (regular data address space) reading is allowed.

Claim 5 is rejected as applied above in rejecting claim 1. Furthermore, Takata discloses:

A semiconductor storage device according to claim 1, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second portion of the regular data stored in the second store in response to the second signal (column 6 lines 7-26).

Claim 13 is rejected as applied above in rejecting claim 9. Furthermore, Takata discloses:

A memory device according to claim 9, wherein the read control circuit includes a comparator for comparing the input address and the dummy address with each other to

output a first signal or a second signal, an enabling/disabling circuit for enabling the first store in response to the first signal and disabling the first store in response to the second signal, and a read address output circuit for outputting a read address for the second portion of the regular data being stored in the second store in response to the second signal (column 6 lines 7-26).

Claim 3 is rejected as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory has a storage capacity larger than the storage capacity of the second regular data storing area, and further includes a dummy address storing area other than the second storing area, for storing the dummy address and the dummy address supplied to the read control circuit is read from the dummy address storing area (column 5 line 59 – column 6 line 26).

Claim 6 is rejecting as applied above in rejecting claim 2. Furthermore, Takata discloses:

A semiconductor storage device according to claim 2, wherein the nonvolatile semiconductor memory and the read control circuit are formed within the same single memory chip (Figure 4, item 30).

Claim 11 is rejected as applied above in rejecting claim 10. Furthermore, Takata discloses:

A memory device according to claim 10, wherein the nonvolatile semiconductor memory has a storage capacity larger than the storage capacity of the second storing area, and further includes a dummy address storing area, other than the second regular data storing area, for storing the dummy address, and the dummy address supplied to the read control circuit is read from the dummy address storing area (column 5 line 59 – column 6 line 26).

Claim 16 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, wherein the nonvolatile semiconductor memory has a storage capacity larger than a storage capacity of the second storing area, and the method further includes storing a dummy address in a dummy address storing area, and reading the dummy address from the dummy address storage area (column 5 line 59 – column 6 line 26).

Claim 17 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including writing to the nonvolatile semiconductor memory with a first write voltage in certain areas thereof, and writing

with a second write voltage lower than the first write voltage in other areas thereof (column 6 lines 55-67).

Claim 18 is rejected as applied above in rejecting claim 15. Furthermore, Takata discloses:

A method according to claim 15, further including comparing the input address and the dummy address with each other to output a first signal or a second signal, and enabling the first storage area in response to the first signal and disabling the first storage area in response to the second signal, and outputting a read address for the second portion of the regular data being stored in the second storage area in response to the second signal (column 5 line 59 – column 6 line 26).

Claim 4 is rejected as applied above in rejecting claim 3. Furthermore, Takata discloses:

A semiconductor storage device according to claim 3, wherein the nonvolatile semiconductor memory is constructed such that the data is written with a first write voltage in the second regular data storing area and the dummy address storing area, and the data is written with a second write voltage lower than the first write voltage in other areas (column 6 lines 55-67).

Claim 12 is rejected as applied above in rejecting claim 11. Furthermore, Takata discloses:

A memory device according to claim 11, wherein the nonvolatile semiconductor memory is constructed such that the data is written in the second game program storing area and the dummy address storing area with a first write voltage and data is written with a second write voltage lower than the first write voltage into other areas, and in the storing area into which the data is written with the second write voltage, backup data representing a development of the game obtained by executing the game program by a processor of a game machine is written (column 6 lines 55-67).

4. Claims 19 – 27 are storage device claims analogous to the storage device claims rejected above, and therefore, are rejected following the same reasoning.

5. Claims 28 – 32 are method claims analogous to the storage device claims rejected above, and therefore, are rejected following the same reasoning.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. Patent No. 5,754,647).

Claim 2 is rejected as applied above in rejecting claim 1. Furthermore, Hsu discloses:

A semiconductor device according to claim 1. Hsu does not explicitly disclose that the first store includes a "masked ROM." However, Hsu discloses a game cartridge, which is well-known to be read-only, or a masked ROM. Therefore, by the nature of the game cartridge, it would have been obvious to one of ordinary skill in the art that the first store storing the regular data (game data) is a masked ROM since the game data is what is meant to be secured, and it would be desirable for the data to be not rewritable.

Claim 10 is rejected as applied above in rejecting claim 9. Furthermore, Hsu discloses:

A memory device according to claim 9. Hsu does not explicitly disclose that the first store includes a "masked ROM." However, Hsu discloses a game cartridge, which is well-known to be read-only, or a masked ROM. Therefore, by the nature of the game cartridge, it would have been obvious to one of ordinary skill in the art that the first store storing the regular data (game data) is a masked ROM since the game data is what is meant to be secured, and it would be desirable for the data to be not rewritable.

Claim 15 is rejected as applied above in rejecting claim 14. Furthermore, Hsu discloses:

The method of claim 14. Hsu does not explicitly disclose that the first store includes a "masked ROM." However, Hsu discloses a game cartridge, which is well-known to be read-only, or a masked ROM. Therefore, by the nature of the game

cartridge, it would have been obvious to one of ordinary skill in the art that the first store storing the regular data (game data) is a masked ROM since the game data is what is meant to be secured, and it would be desirable for the data to be not rewritable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 571-272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary Examiner
AU 2131
8/22/05

KA
08/19/05